

3. (Twice Amended) The method according to claim 23, wherein the metal layer comprises titanium (Ti).

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4. (Twice Amended) The method according to claim 23, wherein the supplemental silicon layer is poly-silicon formed by a CVD (Chemical Vapor Deposition) technique.

5. (Twice Amended) The method according to claim 23, wherein the supplemental silicon layer is a-Si (amorphous silicon) formed by a sputtering technique.

6. (Twice Amended) The method according to claim 23, further comprising:
selectively removing non-reacted silicon from the second-reacted silicide region
after the second annealing.

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23. (Amended) A method for fabricating a semiconductor device, comprising:
providing a semiconductor substrate which has a silicon region located on an insulating layer formed in the semiconductor substrate;
forming a metal layer on the silicon region;
performing a first annealing to form a first-reacted silicide region;
forming a supplemental silicon layer on the first-reacted silicide region; and
performing a second annealing to convert the first-reacted silicide region into a

second-reacted silicide region, by reaction of the supplemental silicon layer with the first-reacted silicide region,

wherein after the second annealing, a silicon layer remains between the second-reacted silicide region and the insulating layer.

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24. (Amended) A method for fabricating a semiconductor device, comprising:
providing a semiconductor substrate which has a silicon region located on an

insulating layer formed in the semiconductor substrate;

forming a metal layer on the silicon region of the semiconductor substrate;

performing a first annealing on the semiconductor substrate to form a first-reacted silicide region;

forming a supplemental silicon layer on the first-reacted silicide region;

doping an impurity into the supplemental silicon layer; and

performing a second annealing to convert the first-reacted silicide region into a second-reacted silicide region, by reaction of the supplemental silicon layer with the first-reacted silicide region,

the semiconductor device including a p-channel MOS transistor having p-type source and drain diffusion layers, and including an n-channel MOS transistor having n-type source and drain diffusion layers,

said doping comprising doping a p-type impurity into the supplemental silicon layer that is formed over the p-channel MOS transistor and doping an n-type impurity

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into the supplemental silicon layer that is formed over the n-channel MOS transistor.

Please add claims 25-29 as follows:

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--25. The method according to claim 24, wherein the metal layer comprises cobalt (Co).

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26. The method according to claim 24, wherein the metal layer comprises titanium (Ti).

27. The method according to claim 24, wherein the supplemental silicon layer is poly-silicon formed by a CVD (Chemical Vapor Deposition) technique.

28. The method according to claim 24, wherein the supplemental silicon layer is a-Si (amorphous silicon) formed by a sputtering technique.

29. The method according to claim 24, further comprising:
selectively removing non-reacted silicon from the second-reacted silicide region
after the second annealing.--